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**Huang et al.**

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(54) **REPLACEMENT CHANNEL**

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(73) Assignee: **Taiwan Semiconductor Manufacturing Co., Ltd.**, Hsin-Chu (TW)

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(22) Filed: **Sep. 8, 2014**

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US 2015/0001584 A1 Jan. 1, 2015

**Related U.S. Application Data**

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(51) **Int. Cl.**

| | |
|---|---|
| ***H01L 29/66*** | (2006.01) |
| ***H01L 29/78*** | (2006.01) |
| ***H01L 29/10*** | (2006.01) |
| ***H01L 29/165*** | (2006.01) |
| ***H01L 29/08*** | (2006.01) |
| ***H01L 29/16*** | (2006.01) |

(52) **U.S. Cl.**

CPC .......... ***H01L 29/785*** (2013.01); ***H01L 29/0847*** (2013.01); ***H01L 29/1037*** (2013.01); ***H01L 29/1054*** (2013.01); ***H01L 29/16*** (2013.01); ***H01L 29/165*** (2013.01); ***H01L 29/6659*** (2013.01); ***H01L 29/66545*** (2013.01); ***H01L 29/66636*** (2013.01); ***H01L 29/66651*** (2013.01); ***H01L 29/7834*** (2013.01); ***H01L 29/7848*** (2013.01)

(58) **Field of Classification Search**

None

See application file for complete search history.

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*Assistant Examiner* — Shaka White
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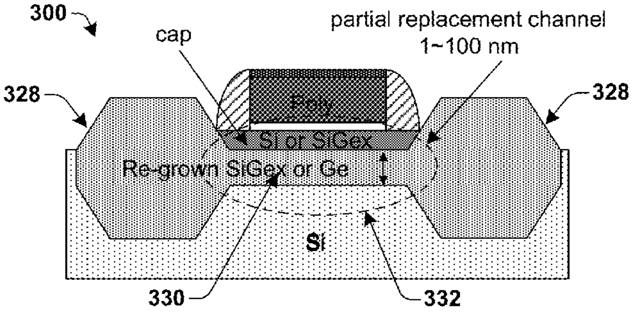
(57) **ABSTRACT**

The present disclosure relates to a device and method for strain inducing or high mobility channel replacement in a semiconductor device. The semiconductor device is configured to control current from a source to a drain through a channel region by use of a gate. A strain inducing or high mobility layer produced in the channel region between the source and drain can result in better device performance compared to Si, faster devices, faster data transmission, and is fully compatible with the current semiconductor manufacturing infrastructure.

**20 Claims, 15 Drawing Sheets**



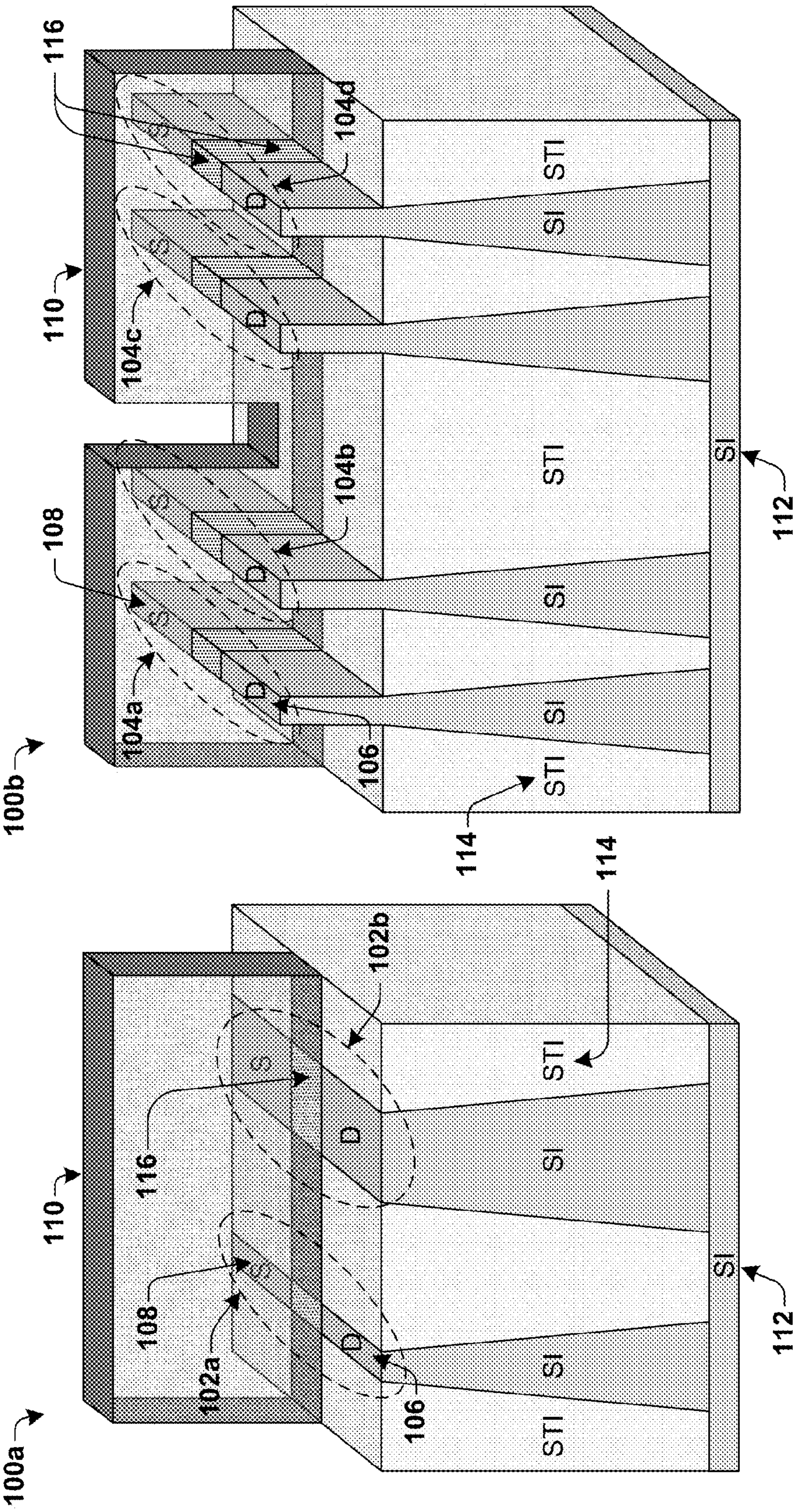

S
D
STI
SI
S
D
STI
SI

Fig. 1

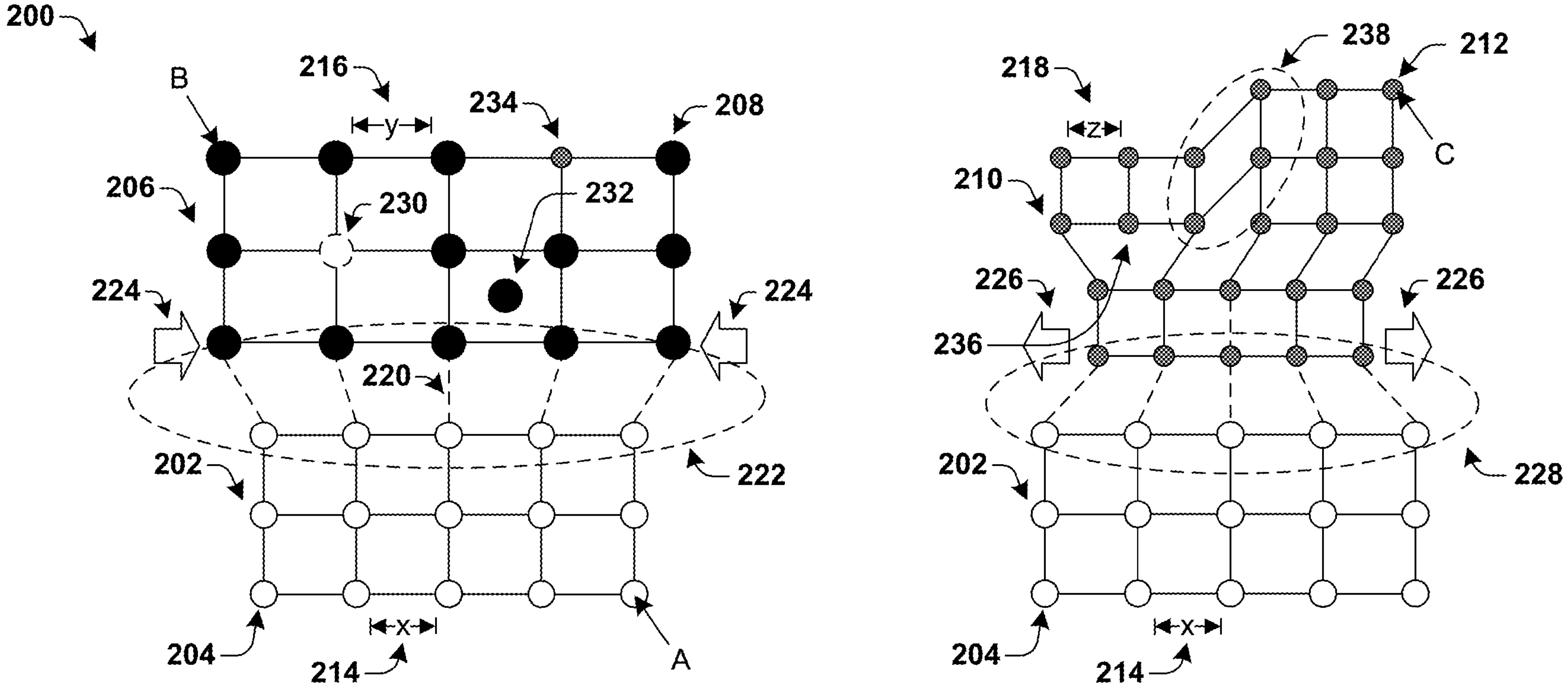

B
y
x
A
z
C
x

Fig. 2

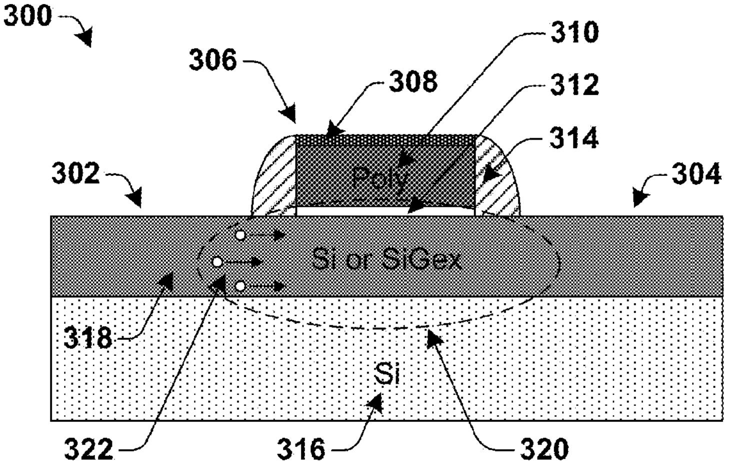

300
306
308
310
312
314
302
304
Poly
Si or SiGex
318
Si
322
316
320

Fig. 3A

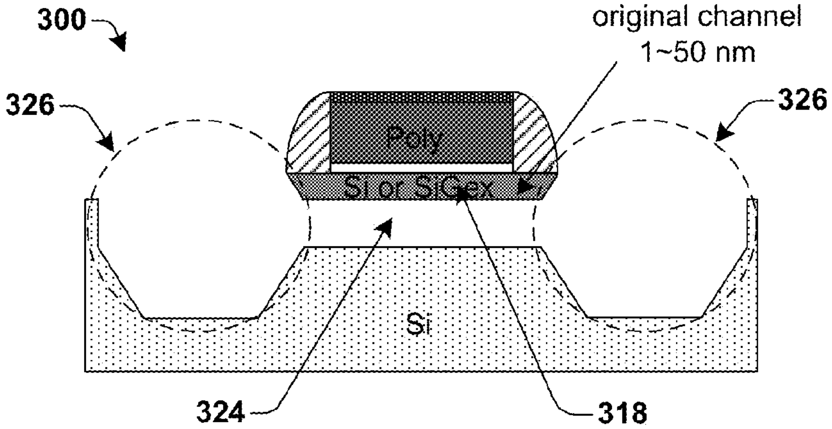

300
original channel
1~50 nm
326
326
Poly
Si or SiGex
Si
324
318

Fig. 3B

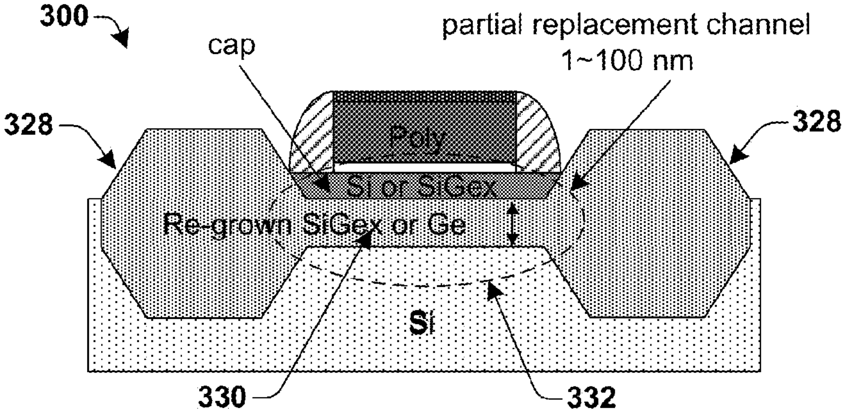

300
cap
partial replacement channel
1~100 nm
328
328
Poly
Si or SiGex
Re-grown SiGex or Ge
Si
330
332

Fig. 3C

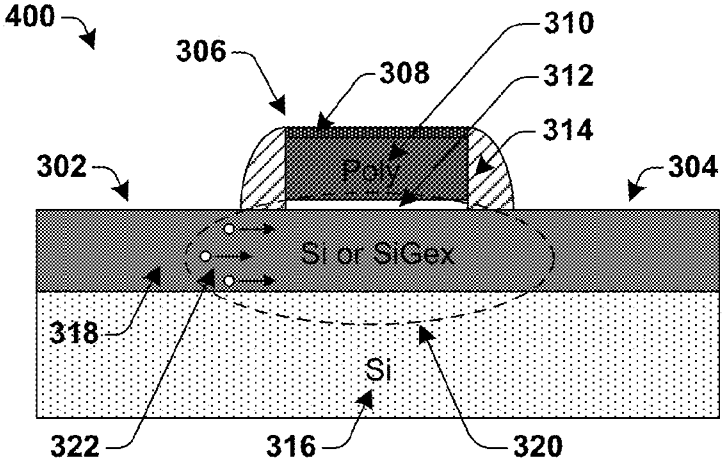

400
306
308
310
312
314
302
304
Poly
Si or SiGex
318
Si
322
316
320

Fig. 4A

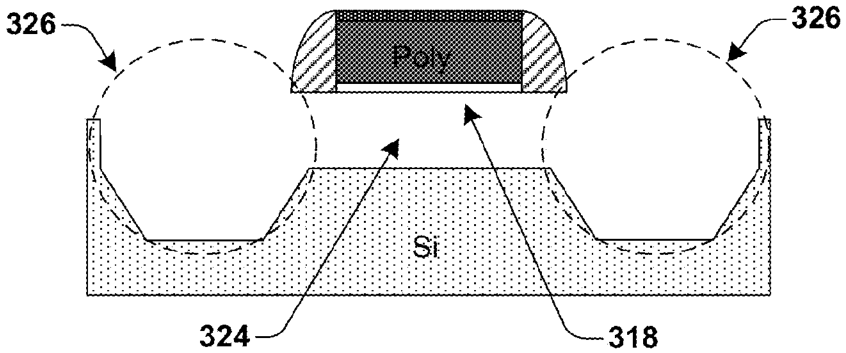

400
326
326
Poly
Si
324
318

Fig. 4B

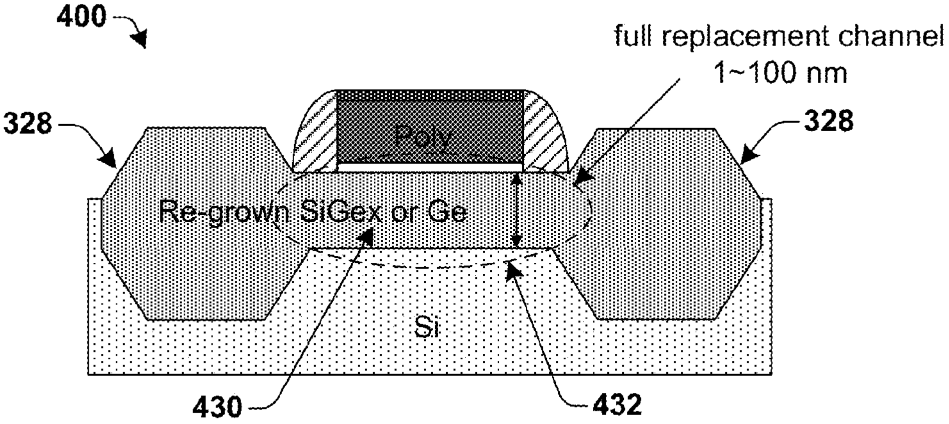

400
full replacement channel
1~100 nm
328
328
Poly
Re-grown SiGex or Ge
Si
430
432

Fig. 4C

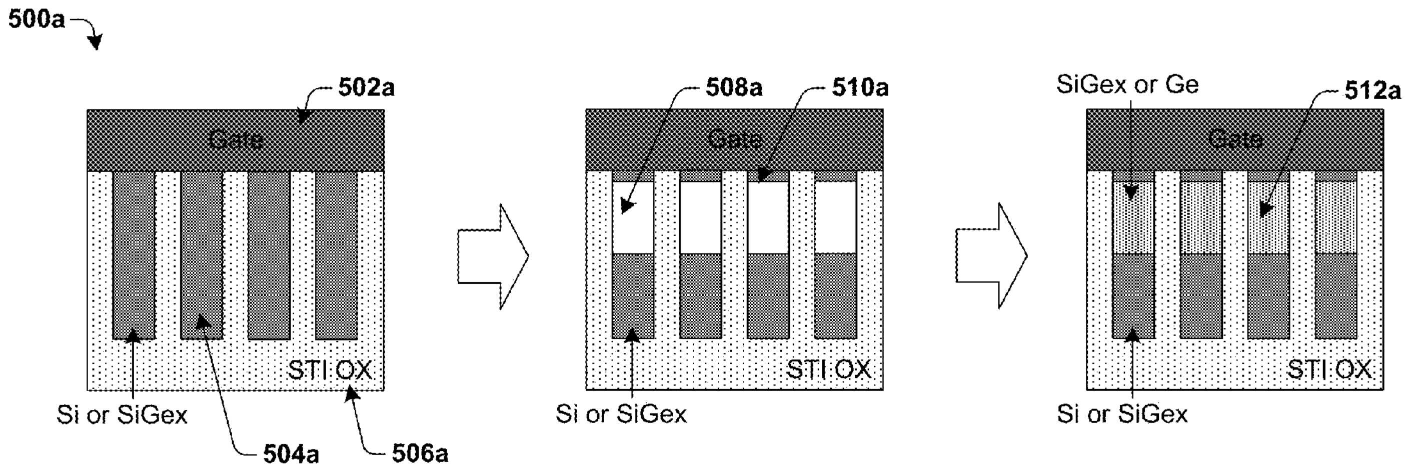

500a
502a
Gate
STI OX
Si or SiGex
504a
506a
508a
510a
Gate
STI OX
Si or SiGex
SiGex or Ge
512a
Gate
STI OX
Si or SiGex

Fig. 5A

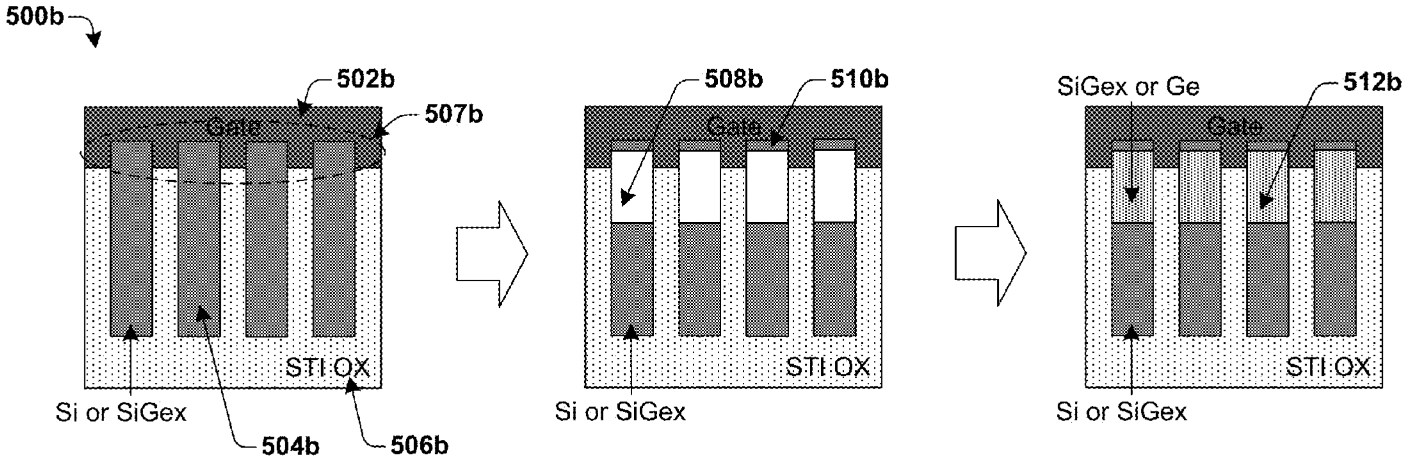

500b
502b
507b
Gate
STI OX
Si or SiGex
504b
506b
508b
510b
Gate
STI OX
Si or SiGex
SiGex or Ge
512b
Gate
STI OX
Si or SiGex

Fig. 5B

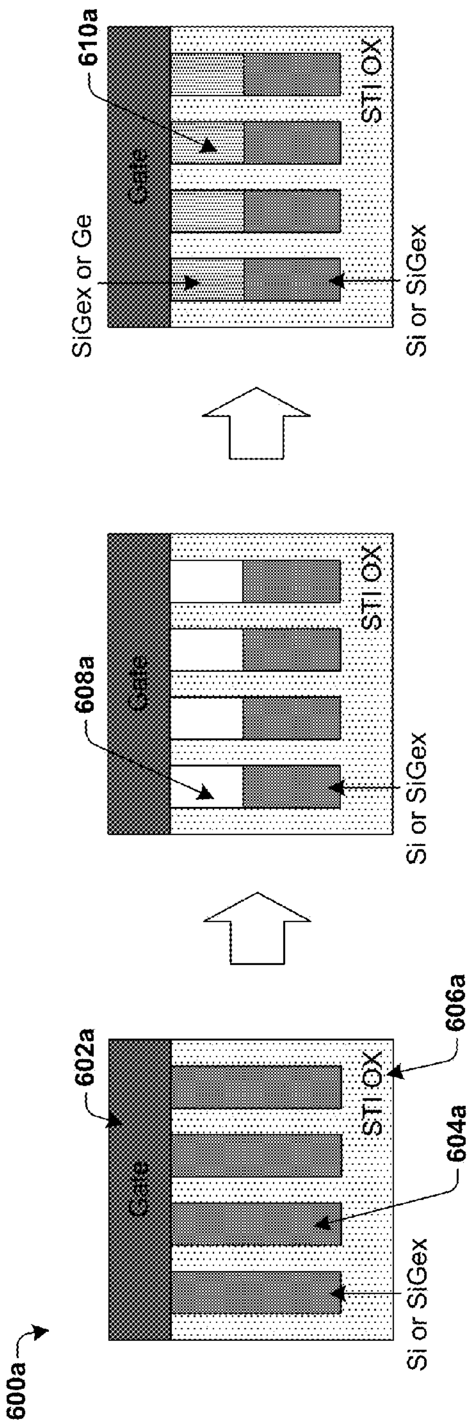

Gate
STI OX
Si or SiGex
SiGex or Ge

Fig. 6A

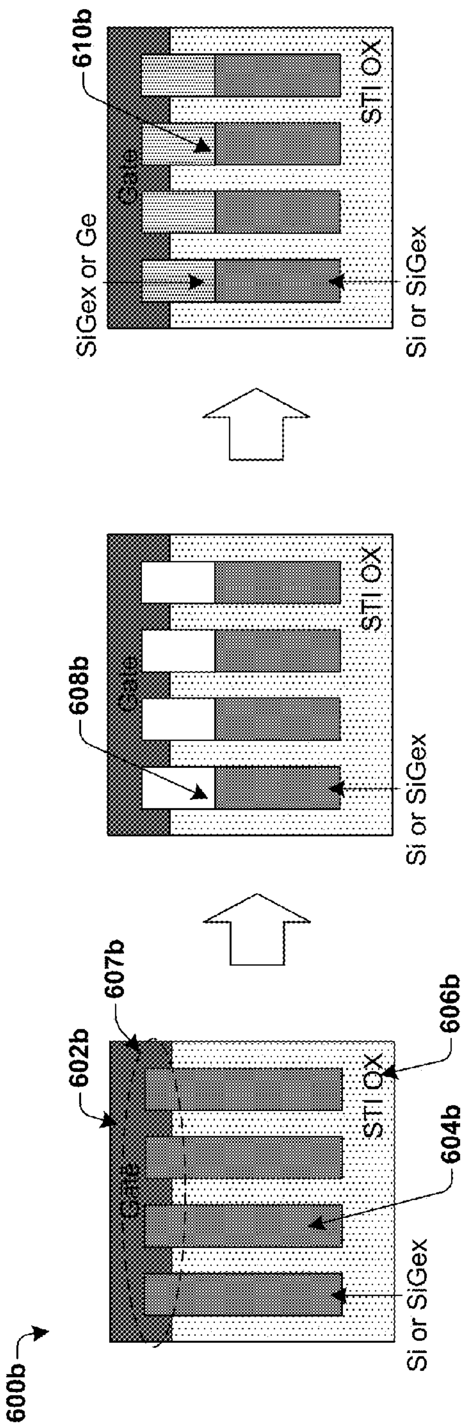

Gate
STI OX
Si or SiGex
SiGex or Ge

Fig. 6B

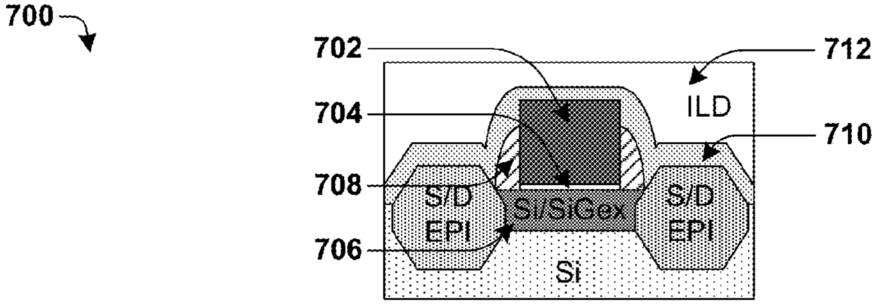

700
702
712
ILD
704
710
708
S/D
EPI
Si/SiGex
S/D
EPI
706
Si

Fig. 7A

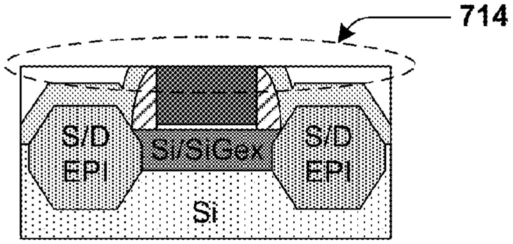

714
S/D
EPI
Si/SiGex
S/D
EPI
Si

Fig. 7B

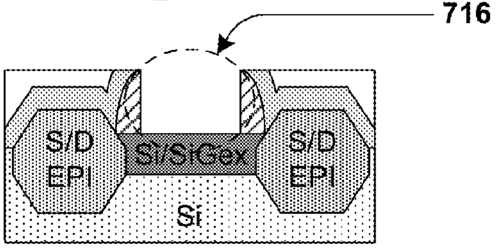

716
S/D
EPI
Si/SiGex
S/D
EPI
Si

Fig. 7C

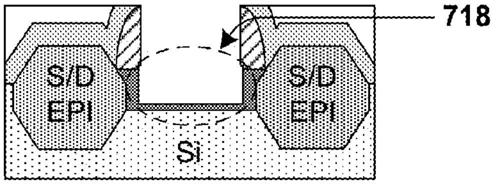

718
S/D
EPI
S/D
EPI
Si

Fig. 7D

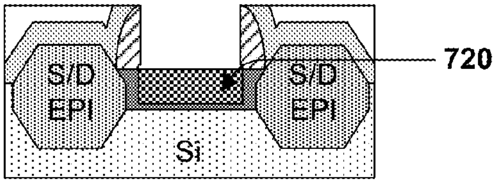

720
S/D
EPI
S/D
EPI
Si

Fig. 7E

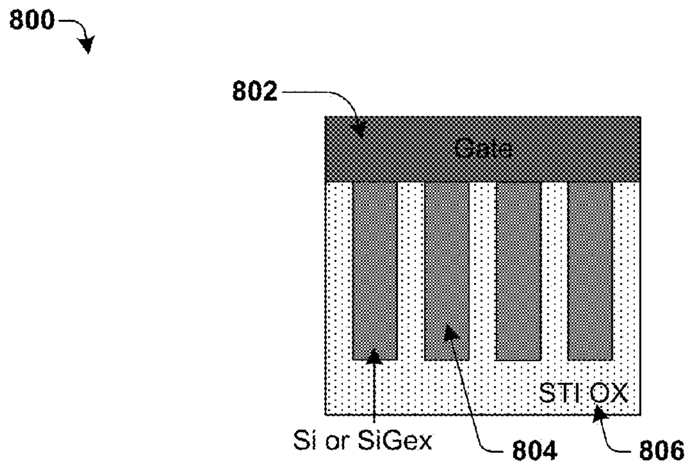

800
802
Gate
STI OX
Si or SiGex
804
806

Fig. 8A

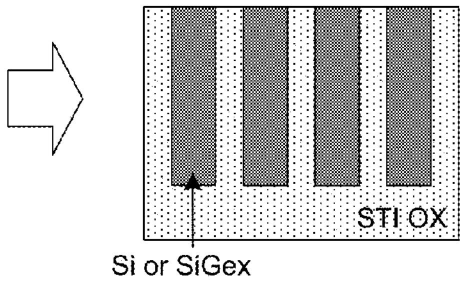

STI OX
Si or SiGex

Fig. 8B

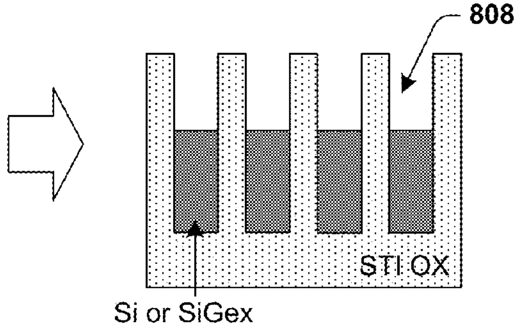

808
STI OX
Si or SiGex

Fig. 8C

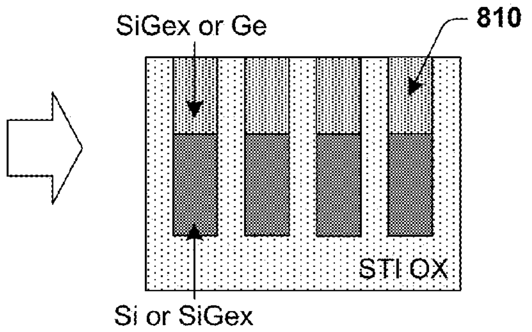

SiGex or Ge
810
STI OX
Si or SiGex

Fig. 8D

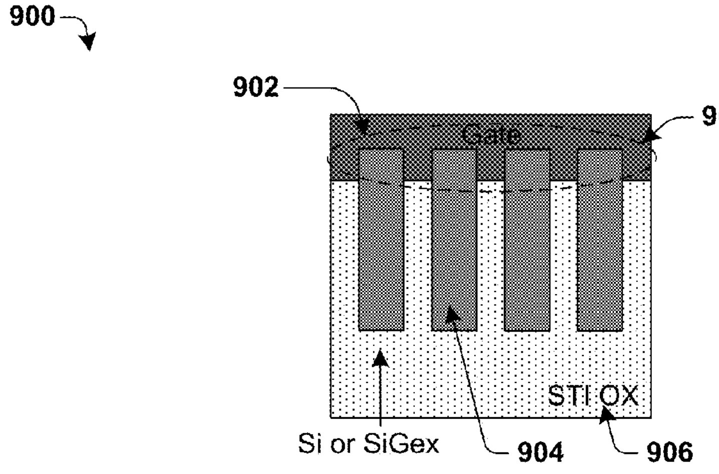

900
902
Gate
908
Si or SiGex
904
STI OX
906

Fig. 9A

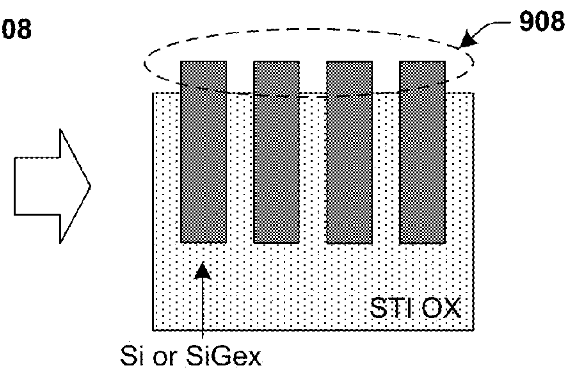

908
STI OX
Si or SiGex

Fig. 9B

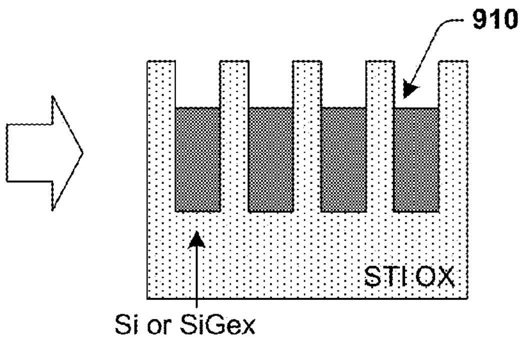

910
STI OX
Si or SiGex

Fig. 9C

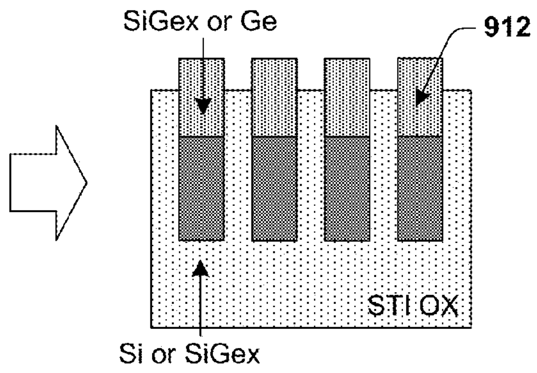

SiGex or Ge
912
STI OX
Si or SiGex

Fig. 9D

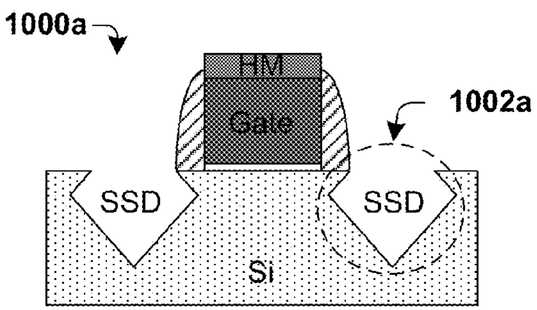

1000a
HM
Gate
1002a
SSD
SSD
Si

Fig. 10A

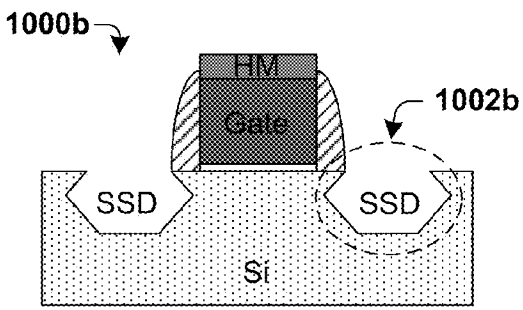

1000b
HM
Gate
1002b
SSD
SSD
Si

Fig. 10B

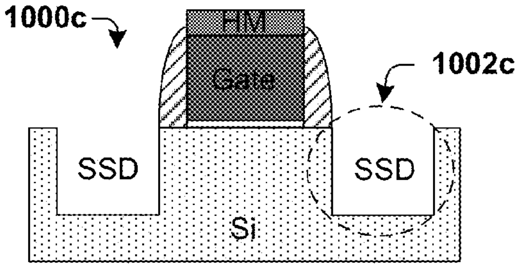

1000c
HM
Gate
1002c
SSD
SSD
Si

Fig. 10C

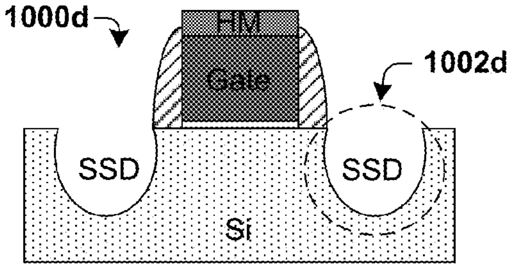

1000d
HM
Gate
1002d
SSD
SSD
Si

Fig. 10D

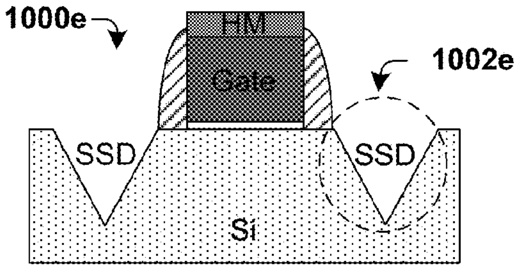

1000e
HM
Gate
1002e
SSD
SSD
Si

Fig. 10E

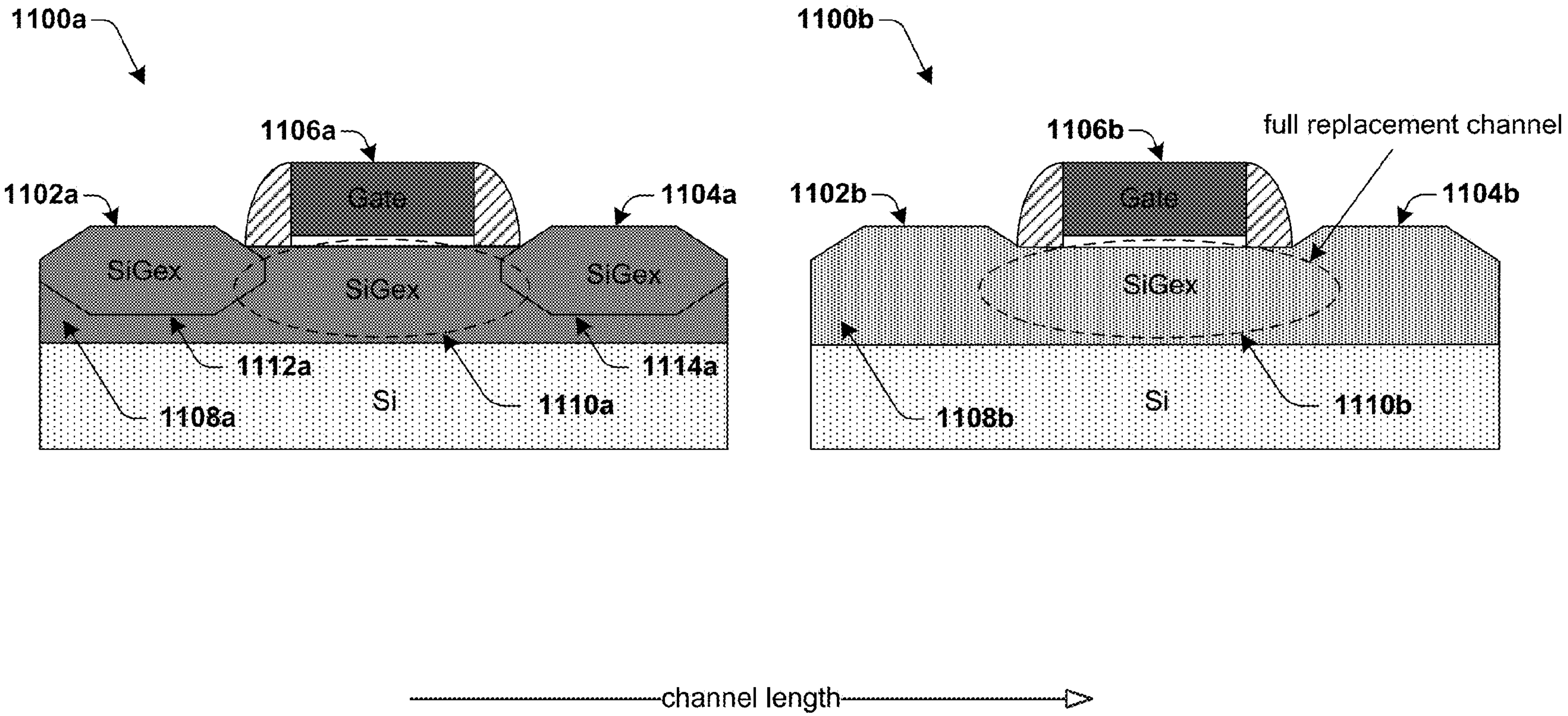

1100a
1106a
Gate
1102a
1104a
SiGex
SiGex
SiGex
1112a
1114a
Si
1108a
1110a
1100b
1106b
Gate
full replacement channel
1102b
1104b
SiGex
Si
1108b
1110b
channel length

Fig. 11

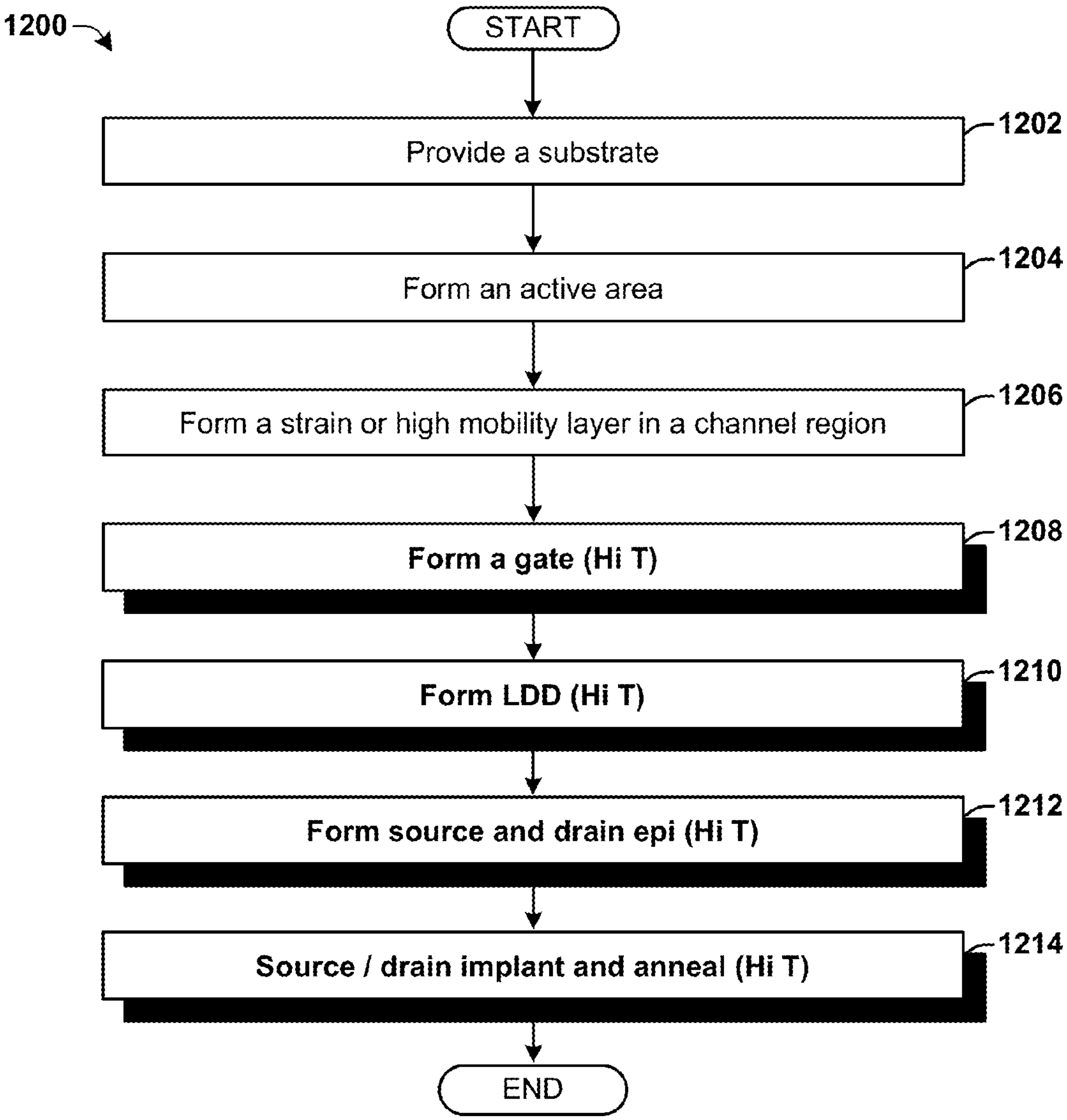

1200
START
Provide a substrate
1202
Form an active area
1204
Form a strain or high mobility layer in a channel region
1206
Form a gate (Hi T)
1208
Form LDD (Hi T)
1210
Form source and drain epi (Hi T)
1212
Source / drain implant and anneal (Hi T)
1214
END

Fig. 12

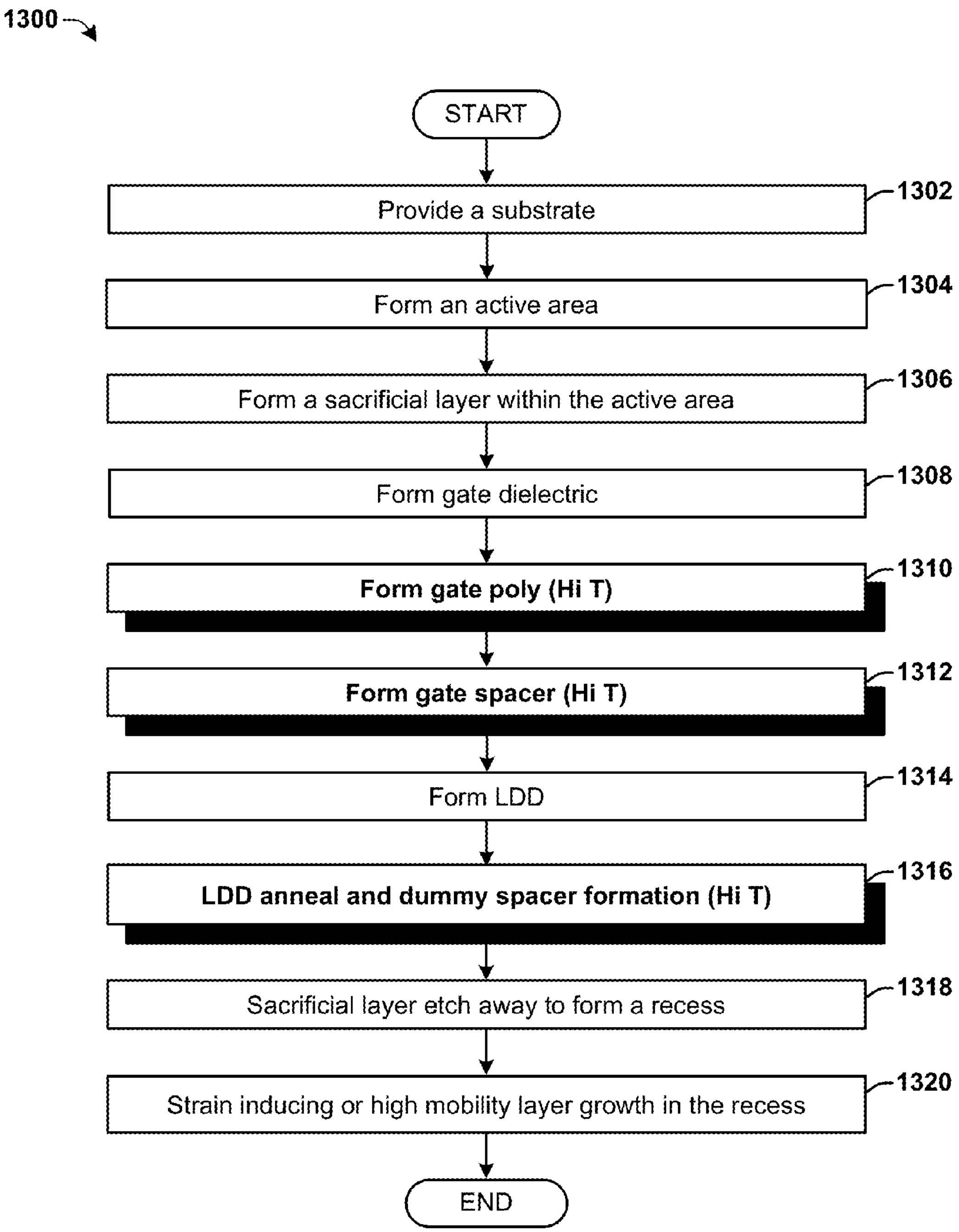

1300
START
Provide a substrate
1302
Form an active area
1304
Form a sacrificial layer within the active area
1306
Form gate dielectric
1308
Form gate poly (Hi T)
1310
Form gate spacer (Hi T)
1312
Form LDD
1314
LDD anneal and dummy spacer formation (Hi T)
1316
Sacrificial layer etch away to form a recess
1318
Strain inducing or high mobility layer growth in the recess
1320
END

Fig. 13

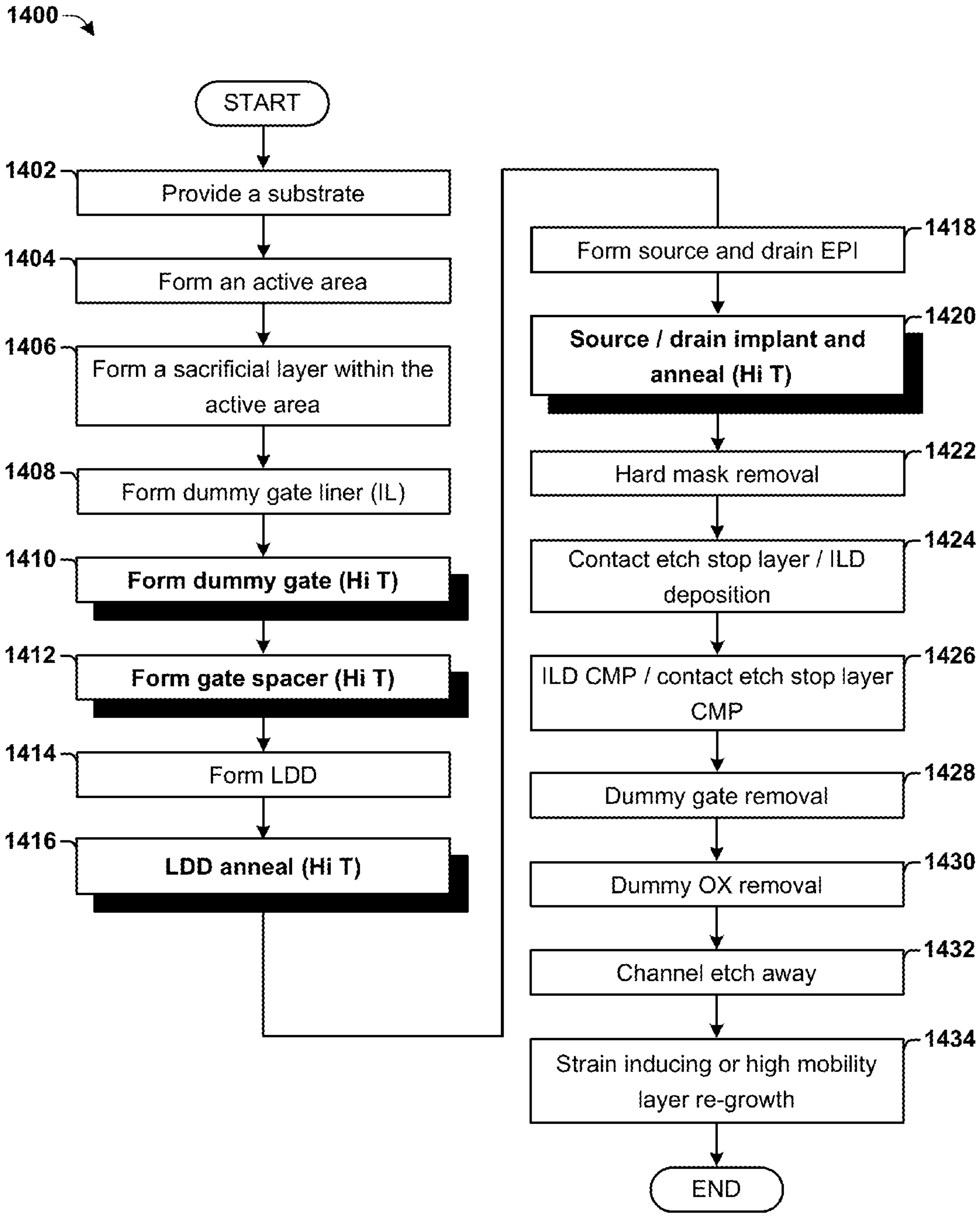

1400
START
1402
Provide a substrate
1404
Form an active area
1406
Form a sacrificial layer within the active area
1408
Form dummy gate liner (IL)
1410
Form dummy gate (Hi T)
1412
Form gate spacer (Hi T)
1414
Form LDD
1416
LDD anneal (Hi T)
1418
Form source and drain EPI
1420
Source / drain implant and anneal (Hi T)
1422
Hard mask removal
1424
Contact etch stop layer / ILD deposition
1426
ILD CMP / contact etch stop layer CMP
1428
Dummy gate removal
1430
Dummy OX removal
1432
Channel etch away
1434
Strain inducing or high mobility layer re-growth
END

Fig. 14

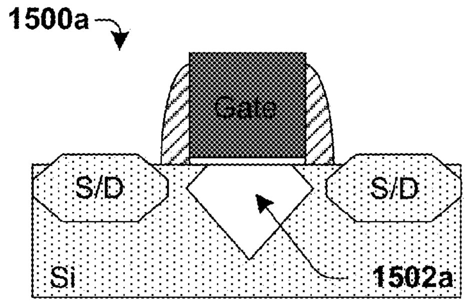

1500a
Gate
S/D
S/D
Si
1502a

Fig. 15A

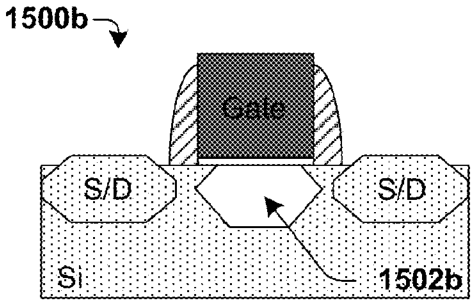

1500b
Gate
S/D
S/D
Si
1502b

Fig. 15B

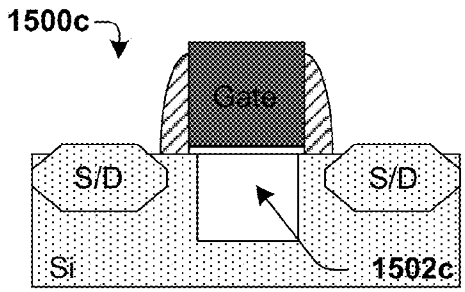

1500c
Gate
S/D
S/D
Si
1502c

Fig. 15C

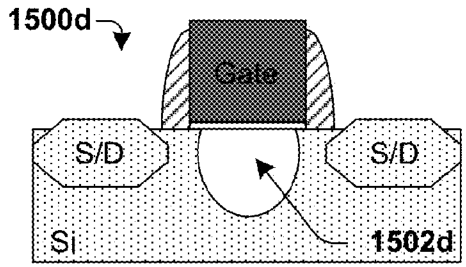

1500d
Gate
S/D
S/D
Si
1502d

Fig. 15D

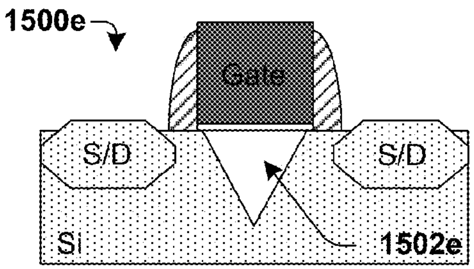

1500e
Gate
S/D
S/D
Si
1502e

Fig. 15E

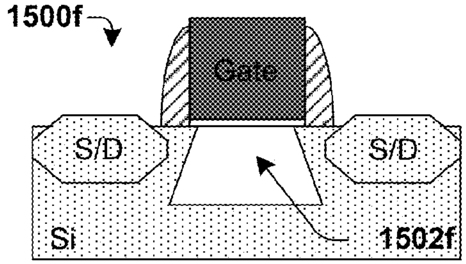

1500f
Gate
S/D
S/D
Si
1502f

Fig. 15F

# REPLACEMENT CHANNEL

## REFERENCE TO RELATED APPLICATION

This application is a continuation of U.S. application Ser. No. 13/446,375 filed on Apr. 13, 2012.

## BACKGROUND

The cost and complexity associated with scaling of semiconductor device sizes according to Moore's law has given rise to new methods to improve semiconductor device characteristics. New gate materials such as Hi-K metal gates to decrease device leakage, finFET devices with increased effective gate area as compared to same-size planar devices, and strain inducing channels for increased charge carrier mobility are a few examples of methods to continue Moore's Law scaling for next generation microprocessor designs.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** illustrates semiconductor devices with strain inducing channels formed by conventional methods.

FIG. **2** illustrates some embodiments of strained lattices.

FIG. **3**A-FIG. **3**C illustrate some embodiments of forming a p-type metal-oxide semiconductor field transistor (p-MOS) transistor with a partial replacement channel.

FIG. **4**A-FIG. **4**C illustrate some embodiments of forming a p-type metal-oxide semiconductor field transistor (p-MOS) transistor with a full replacement channel.

FIG. **5**A illustrates some embodiments of forming a partial replacement channel on planar FETs.

FIG. **5**B illustrates some embodiments of forming a partial replacement channel on finFETs.

FIG. **6**A illustrates some embodiments of forming a full replacement channel on planar FETs.

FIG. **6**B illustrates some embodiments of forming a full replacement channel on finFETs.

FIG. **7**A-FIG. **7**E illustrate some detailed embodiments of forming a channel-last replacement channel on a planar FET in a Hi-K metal gate last (HKL) flow.

FIG. **8**A-FIG. **8**D illustrate some embodiments of forming a channel-last replacement channel on planar FETs in a Hi-K metal gate last (HKL) flow.

FIG. **9**A-FIG. **9**D illustrate some embodiments of forming a channel-last replacement channel on finFETs in a Hi-K metal gate last (HKL) flow.

FIG. **10**A-FIG. **10**E illustrate cross-sectional views of some embodiments of typical SSD etch profiles.

FIG. **11** illustrates a comparison of some embodiments of a p-MOS formed by conventional strain inducing channel methods vs. a p-MOS formed by a full replacement channel method.

FIG. **12** illustrates a flow diagram of some embodiments of a conventional method for manufacturing a strain inducing or high mobility channel.

FIG. **13** illustrates a flow diagram of some embodiments of a method for manufacturing a replacement channel that can be used for both a partial replacement channel and a full replacement channel.

FIG. **14** illustrates a flow diagram of some embodiments of a method for manufacturing a channel-last replacement channel.

FIG. **15**A-FIG. **15**F illustrate cross-sectional views of some embodiments of channel-last replacement channel profiles.

## DETAILED DESCRIPTION

The description herein is made with reference to the drawings, wherein like reference numerals are generally utilized to refer to like elements throughout, and wherein the various structures are not necessarily drawn to scale. In the following description, for purposes of explanation, numerous specific details are set forth in order to facilitate understanding. It may be evident, however, to one of ordinary skill in the art, that one or more aspects described herein may be practiced with a lesser degree of these specific details. In other instances, known structures and devices are shown in block diagram form to facilitate understanding.

FIG. **1** illustrates semiconductor devices with strain inducing channels formed by conventional methods, comprising an arrangement **100***a* of two planar field-effect transistors (FETs) **102***a* and **102***b*, as well as an arrangement **100***b* of four fin field-effect transistors (finFETs) **104***a*-**104***d*. Each FET **102***a*-**102***b* and finFET **104***a*-**104***d* comprise three terminals: a source **106**, a drain **108**, and a gate **110**, and are formed on a silicon (Si) substrate **112** and isolated by shallow trench isolation (STI) channels **114** filled with a dielectric material (e.g., $SiO_2$). Planar FETs **102***a*-**102***b* and finFETs **104***a*-**104***d* typically comprises a metal-oxide-semiconductor FETs (MOSFETs) wherein a Hi-K dielectric resides between the gate **110** and a channel region **116** formed between each source **106** and drain **108** to reduce power loss due to gate current leakage into the channel region **116**.

One factor in determining the performance of a FET is the mobility of charge carriers through the channel region **116**. To increase the mobility of charge carriers in a FET, a strain inducing channel may be produced. However, strain inducing channels formed by conventional methods are formed early in semiconductor processing, and may be subject to a series of thermal processing steps which can degrade their crystal structure and hence reduce their charge carrier mobility.

Accordingly, the present disclosure relates to a device and method for strain inducing or high mobility channel replacement in a semiconductor device. A sacrificial layer is formed early in the semiconductor device processing. After one or more thermal processing steps are carried out with the sacrificial layer in place, the sacrificial layer is removed to form a recess. A strain inducing or high mobility layer then fills the recess to insure a robust crystal structure with minimal defects. Strain inducing or high mobility channel replacement may result in better device performance compared to conventional techniques for strain inducing channel formation, and is fully compatible with the current semiconductor manufacturing infrastructure.

FIG. **2** illustrates some embodiments of strained lattices **200** which are used in semiconductor devices due to their relatively high charge carrier mobility. The strained lattices **200** comprise a first lattice **202** composed of species A **204**, a second lattice **206** composed of species B **208**, and a third lattice **210** composed of species C **212**. The periodic spacing of a species within a given lattice is defined as its lattice constant. The first lattice **202** has a lattice constant x **214**, the second lattice **206** has a lattice constant y **216**, and the third lattice **210** has a lattice constant z **218**. Near the interface region **222** of the first lattice **202** and the second lattice **206** a mismatch in lattice constants results in a strain of one or more of the first or second crystal lattices, **202** and **206** respectively. In this embodiment, the second lattice **206** is subject to a compressive strain **224** resulting a mismatch of its lattice constant y with the lattice constant x **214** (i.e., y>x results in compressive strain **224** for the second lattice **206**). Similarly, the third lattice **210** is subject to a tensile strain **226** resulting from a mismatch of its lattice constant z with the lattice constant x **214** near the interface **228** (i.e., z<x results in tensile strain **226** for the third lattice **210**).

Mechanical strain, thermal effects, and chemical effects are some examples of factors that can result in defects within a lattice. A vacancy **230** results from a particle of species A **204** being absent from its expected periodic location. An Interstitial **232** results from a particle of species A **204** being in a location other than its expected periodic location. A substitution **234** results from a particle of species C **212** residing in a location where a particle of species A **204** is expected (e.g., a contaminant for a single-species lattice). An edge dislocation **236** is where an extra half plane of particles is introduced. A stacking fault **238** occurs when one or more planes of atoms interrupts the normal periodic stacking of particle planes. These defects degrade the crystal structure and hence the charge carrier mobility of these strained lattices. Moreover, as defects accumulate the crystal structure may become so distorted that it becomes amorphous.

To improve the strain within a strain inducing layer when thermal processing steps are used in semiconductor device processing a sacrificial layer may be formed early in the semiconductor device processing. After one or more thermal processing steps are carried out with the sacrificial layer in place, the sacrificial layer is removed to form a recess. A strain inducing or high mobility layer then fills the recess to insure a robust crystal structure with minimal defects.

FIG. **3***a*-FIG. **3***c* illustrate some embodiments of forming a p-type metal-oxide semiconductor field transistor (p-MOS) transistor with a partial replacement channel. FIG. **3***a* illustrates p-MOS **300** comprising a source **302**, a drain **304**, and a gate **306**. The gate **306** comprises a hard mask **308**, Poly-Silicon gate material (Poly-Si) **310**, a gate dielectric **312**, and sidewall spacers **314** to insure electrical isolation of the gate **306** from the source **302** and drain **304**. The p-MOS **300** is situated on a Si substrate **316** (i.e., Si lattice) to which a sacrificial layer of Si or SiGe **318** has been added (i.e., SiGex where x≥0.2). The sacrificial layer of Si or SiGe **318** forms a channel region **320** through which hole charge carriers **322** move from the source **302** to the drain **304**. The mismatch in lattice constants between the Si substrate **316** and combined Si or SiGe **318** results in a compressive strain within the channel region **320** of the p-MOS **300** along the channel width direction, having the effect of increasing the hole charge carrier **322** mobility by approximately 1.4-1.8 times that of bulk devices (i.e., Si).

The hole charge carrier **322** mobility, however, will be degraded by thermal processing steps that occur after the formation of the sacrificial layer of Si or SiGe **318**, due to the distortion its lattice structure. FIG. **3***b* illustrates the p-MOS **300** wherein the sacrificial Si or SiGe layer **318** has been etched away (e.g., a wet chemical etch, a dry chemical etch, or a combination thereof) to form a recess **324** after the thermal processing steps are complete. At the same time (i.e., as a part of the same etch step) a strained source drain (SSD) etch forms larger etch profile regions **326** within the recess. Note that a portion of the sacrificial layer of Si or SiGe **318** approximately 1-50 nm thick remains below the gate **306**, and shields the gate **306** from any undesired effects from removing the sacrificial layer of Si or SiGe **318** (e.g., damage and/or contamination).

FIG. **3***c* illustrates the p-MOS **300** wherein the recess **324** has been filled with a single strain inducing or high mobility layer **330** (i.e., single lattice) comprising SiGex (where x≥0.2) or Ge with a gradient concentration, either doped or undoped, with a cap formed from the sacrificial layer of Si or SiGe **318** that remains below the gate **306**. This method of replacement results in a partial replacement channel **332** and source drain regions **328** comprising a single crystal. While formation of a partial replacement channel **332** has the benefit of protecting the gate **306**, it results in less overall strain and hence less hole mobility than a full replacement channel. Nonetheless, because the partial replacement channel **332** comprises a strain induced layer formed after thermal processing, it has an increased induced-strain relative to conventional devices.

A strain inducing channel on an n-type metal-oxide semiconductor field transistor (n-MOS) can be achieved by the same means as described in the embodiments of the p-MOS **300** wherein a composite layer of strained Si on strained SiGe (e.g., Si/SiGe$_{0.2}$) fills the recess **324** instead of the strain inducing or high mobility layer **330**. The mismatch in lattice constants between the composite layer of strained Si on strained SiGe and the substrate **316** results in a tensile strain of the n-MOS along the channel width direction, having the effect of increasing the electron charge carrier mobility by approximately 1.25-2 times that of bulk devices.

FIG. **4***a*-FIG. **4***c* illustrate some embodiments of forming a p-type metal-oxide semiconductor field transistor (p-MOS) transistor with a full replacement channel. The formation of a full replacement channel illustrated for a p-MOS **400** in FIG. **4***a*-**4***c* is similar to the formation of the partial replacement channel described in the embodiments of FIG. **3***a*-FIG. **3***c*. However, for the formation of a full replacement channel, no portion of the sacrificial layer of Si or SiGe **318** remains such that the recess **324** abuts the bottom of the gate dielectric **312**. The recess **324** is then filled with a single strain inducing or high mobility layer **430** (i.e., single lattice) comprising SiGex (where x≥0.2) or Ge with a gradient concentration, and is either doped or undoped. Note that no cap is formed since the sacrificial layer of Si or SiGe **318** has been completely removed. The strain inducing or high mobility layer **430** forms the source **302**, drain **304**, and a full replacement channel **432**, which results in more overall strain than the partial replacement channel, and hence an increased hole mobility relative to the partial replacement channel.

FIG. **5***a* illustrates some embodiments of forming a partial replacement channel on planar FETs **500***a*. Note that the cross-section shown for this embodiment is rotated **90** degrees from the embodiments of FIG. **3** and FIG. **4** such that the channel length direction faces out of the page. The planar FETs **500***a* comprise a gate **502***a*, and Si or SiGex channels **504***a* which are isolated from one another by a shallow trench isolation oxide (STI OX) **506***a*. Each original channel of Si or SiGe is etched away (e.g., a wet chemical etch, a dry chemical etch, or a combination thereof) to form a recess **508***a*, leaving a portion of the Si or SiGe channel **510***a* approximately 1-50 nm thick below the gate **502***a*. A strain inducing layer or high mobility layer **512***a* of SiGex (where x≥0.2) or Ge is then re-grown within the recess **508***a* (e.g., epitaxial growth). This method results in the formation of a partial replacement channel on the planar FETs **500***a*.

FIG. **5***b* illustrates some embodiments of forming a partial replacement channel on finFETs **500***b*, which is identical to the embodiments of forming a partial replacement channel on planar FETs **500***a* with the distinction that the Si or SiGex channels **504***b* extend into the gate **502***b* to form "fins" **507***b* that are wrapped in by the gate **502***b* on three sides. Each Si or SiGex channel **504***b* is etched away to form a recess **508***b* with a portion of the Si or SiGe channel **510***b* approximately 1-50 nm thick remaining at the top of the original Si or SiGex channel **504***b*. A strain inducing layer or high mobility layer **512***b* of SiGex (where x≥0.2) or Ge is then re-grown within the recess **508***b*. This method results in the formation of a partial replacement channel on the finFETs **500***b*.

FIG. **6***a* illustrates some embodiments of forming a full replacement channel on planar FETs **600***a*, which comprise a gate **602***a*, and Si or SiGex channels **604***a* which are isolated from one another by a shallow trench isolation oxide (STI OX) **606***a*. Each original channel of Si or SiGe is etched away to form a recess **608***a* such that no portion of the Si or SiGe channel **604***a* resides between the recess **608***a* and the gate **602***a* (i.e., the recess abuts the bottom of the gate). A strain inducing layer or high mobility layer **610***a* of SiGex (where x≥0.2) or Ge is then re-grown within the recess **608***a*. This method results in the formation of a full replacement channel on the planar FETs **600***a*.

FIG. **6***b* illustrates some embodiments of forming a full replacement channel on finFETs **600***b*. The distinction between the embodiments of **600***a* and **600***b* is similar to the distinction between the embodiments of **500***a* and **500***b*, wherein the only difference is that the Si or SiGex channels **604***b* extend into the gate **602***b* to form "fins" **607***b* that are wrapped in by the gate **602***b* on three sides. Each Si or SiGe channel is etched away to form a recess **608***b* which abuts the bottom of the gate **602***b*. A strain inducing layer or high mobility layer **610***b* of SiGex (where x≥0.2) or Ge is then re-grown within the recess **608***b* to form a full replacement channel on the finFETs **600***b*.

FIG. **7***a*-FIG. **7***e* illustrate some detailed embodiments of forming a channel-last replacement channel on a planar FET **700** in a Hi-K metal gate last (HKL) flow. In the Hi-K metal gate last flow a dummy poly gate and dummy liner (IL) are formed early in the semiconductor device processing and then replaced with a real gate late in the processing. In contrast, a Hi-K metal gate first (HKF) flow forms the real gate early in the processing.

FIG. **7***a* illustrates a cross-sectional view of a planar FET **700** comprising a dummy gate **702**, a dummy liner (IL) **704**, a Si or SiGex (where x≥0.2) channel **706**, a spacer **708**, and a contact etch stop layer **710** formed between the dummy gate **702** and spacer **708** and an interlayer dielectric (ILD) **712**. FIG. **7***b* illustrates a cross-sectional view of the planar FET **700** wherein a chemical-mechanical polish (CMP) **714** has removed the contact etch stop layer **710** and ILD **712** to expose the top of the dummy gate **702**. FIG. **7***c* illustrates a cross-sectional view of the planar FET **700** wherein the dummy gate **702** and the dummy IL **704** have been etched away to form a first recess **716**. FIG. **7***d* illustrates a cross-sectional view of the planar FET **700** wherein the Si or SiGex channel **706** has been etched away to form a second recess **718**. FIG. **7***e* illustrates a cross-sectional view of the planar FET **700** wherein a strain inducing layer or high mobility layer **720** of SiGex (where x≥0.2) or Ge is re-grown within the second recess **718** to form a channel-last replacement channel.

FIG. **8***a*-FIG. **8***d* illustrate some embodiments of forming a channel-last replacement channel on planar FETs **800** in a Hi-K metal gate last (HKL) flow. FIG. **8***a* illustrates a cross-sectional view of the planar FETs **800**, which comprise a dummy gate **802**, and Si or SiGex channels **804** which are isolated from one another by a shallow trench isolation oxide (STI OX) **806**. FIG. **8***b* illustrates a cross-sectional view of the planar FET **800** wherein the dummy gate **802** has been etched away. FIG. **8***c* illustrates a cross-sectional view of the planar FET **800** wherein each original Si or SiGe channel **804** is etched away to form a recess **808**. FIG. **8***d* illustrates a cross-sectional view of the planar FET **800** wherein a strain inducing layer or high mobility layer **810** of SiGex (where x≥0.2) or Ge is then re-grown within the recess **808** to form a channel-last replacement channel.

FIG. **9***a*-FIG. **9***d* illustrate some embodiments of forming a channel-last replacement channel on finFETs **900** in a Hi-K metal gate last (HKL) flow. The distinction between the embodiments of FIG. **8***a*-FIG. **8***d* and FIG. **9***a*-FIG. **9***d* is similar to the distinction between the previous embodiments of **600***a* and **600***b* wherein the only difference is that the Si or SiGex channels **904** extend into the dummy gate **902** to form "fins" **908** as illustrated in a cross-sectional view in FIG. **9***a*. FIG. **9***b* illustrates a cross-sectional view of the finFET **900** wherein the dummy gate **902** has been etched away to expose the Si or SiGex "fins" **908**. FIG. **9***c* illustrates a cross-sectional view of the finFET **900** wherein each original Si or SiGe channel **904** is etched away to form a recess **910**. FIG. **9***d* illustrates a cross-sectional view of the finFET **900** wherein a strain inducing layer or high mobility layer **912** of SiGex (where x≥0.2) or Ge is then re-grown within the recess **910** to form a channel-last replacement channel.

FIG. **10***a*-FIG. **10***e* illustrate cross-sectional views of some embodiments of typical SSD etch profiles. FIG. **10***a* illustrates a cross-sectional view of some embodiments **1000***a* of a sigma-shape etch profile **1002***a* for a strained source drain (SSD) etch. FIG. **10***b* illustrates a cross-sectional view of some embodiments **1000***b* of a sigma-shape etch profile **1002***b* for a strained source drain (SSD) etch. FIG. **10***c* illustrates a cross-sectional view of some embodiments **1000***c* of an anisotropic etch profile **1002***c* for a strained source drain (SSD) etch. FIG. **10***d* illustrates a cross-sectional view of some embodiments **1000***d* of an isotropic etch profile **1002***d* for a strained source drain (SSD) etch. FIG. **10***e* illustrates a cross-sectional view of some embodiments **1000***e* of a triangular etch profile **1002***e* for a strained source drain (SSD) etch.

FIG. **11** illustrates a comparison of some embodiments of a p-MOS **1100***a* formed by conventional strain inducing channel methods vs. a p-MOS **1100***b* formed by a full replacement channel method. The p-MOS **1100***a* formed by a conventional methods comprises a source **1102***a* and drain **1104***a* comprising first and second strained EPI layers of SiGe, respectively. The p-MOS **1100***a* further comprises gate **1106***a*, and a third strained layer of SiGe **1108** that forms a channel region **1110***a*. A first boundary **1112***a* separates the first strained EPI layer of SiGe of the source **1102***a* from the third strained layer of SiGe **1108**. A second boundary **1114***a* separates the second strained EPI layer of SiGe of the drain **1104***a* from the third strained layer of SiGe **1108**. The shape of the first and second boundaries **1112***a*, **1114***a* is determined by the type of strained source drain (SSD) etch used to form the source **1102***a* and drain **1104***a*, and may comprise a sigma-shape profile (shown), an anisotropic etch profile, or an isotropic etch profile. The p-MOS **1100***b* also comprises a source **1102***b*, a drain **1104***b*, and a gate **1106***b*. However, the p-MOS **1100***b* comprises only a single layer of SiGe **1108***b* (i.e., single lattice) that forms the source **1102***b*, drain **1104***b*, as well as a full replacement channel **1110***b*.

FIG. **12** illustrates a flow diagram of some embodiments of a method **1200** for manufacturing a strain inducing or high mobility channel. Note that the method **1200** is applicable in both the Hi-K metal gate last (HKL) flow as well as the Hi-K metal gate first (HKF) flow. While method **1200** is illustrated and described below as a series of acts or events, it will be appreciated that the illustrated ordering of such acts or events are not to be interpreted in a limiting sense. For example, some acts may occur in different orders and/or concurrently with other acts or events apart from those illustrated and/or described herein. In addition, not all illustrated acts may be required to implement one or more aspects or embodiments of the description herein. Further, one or more of the acts depicted herein may be carried out in one or more separate acts and/or phases.

At step **1202** a substrate is provided. The substrate may comprise a 300 mm or 450 mm crystalline wafer comprising silicon that has been doped with boron, phosphorus, arsenic, or antimony.

At step **1204** an active area is formed, which may comprise doping of the substrate.

At step **1206** a strain or high mobility layer is formed in a channel region within the active area.

At step **1208** a gate is formed. The gate may comprise a layer of Poly-Silicon above a layer of gate dielectric, and subjects the substrate to thermal processing (Hi T).

At step **1210** a lightly-doped drain (LDD) is formed to improve charge carrier movement from the source to the drain. Formation of the LDD subjects the substrate to thermal processing (Hi T). The thermal processing may comprise a plurality of high temperature anneals, a plurality of high temperature process steps, or a combination thereof.

At step **1212** a source and drain epi layer is formed. The source and drain epi layer may comprise a layer of epitaxial SiGe for a p-MOS (e.g., $SiGe_{0.3}$), or a composite layer of epitaxial Si on layer of epitaxial SiGe for an n-MOS (e.g., $Si/SiGe_{0.2}$). Formation of the source and drain epi layer subjects the substrate to thermal processing (Hi T). The thermal processing may comprise a plurality of high temperature anneals, a plurality of high temperature process steps, or a combination thereof.

At step **1214** a source and drain implant and anneal is performed. The source and drain implant may comprise an ion implantation of arsenic to improve threshold voltage, and subjects the substrate to thermal cycling (Hi T). The thermal processing may comprise a plurality of high temperature anneals, a plurality of high temperature process steps, or a combination thereof.

FIG. **13** illustrates a flow diagram of some embodiments of a method **1300** for manufacturing a replacement channel that can be used for both a partial replacement channel and a full replacement channel. Note that the method **1300** is applicable in both the Hi-K metal gate last (HKL) flow as well as the Hi-K metal gate first (HKF) flow. While method **1300** is illustrated and described below as a series of acts or events, it will be appreciated that the illustrated ordering of such acts or events are not to be interpreted in a limiting sense. For example, some acts may occur in different orders and/or concurrently with other acts or events apart from those illustrated and/or described herein. In addition, not all illustrated acts may be required to implement one or more aspects or embodiments of the description herein. Further, one or more of the acts depicted herein may be carried out in one or more separate acts and/or phases.

At step **1302** a substrate is provided. The substrate may comprise a 300 mm or 450 mm crystalline wafer comprising silicon that has been doped with boron, phosphorus, arsenic, or antimony.

At step **1304** an active area is formed, which may comprise doping of the substrate.

At step **1306** a sacrificial layer is formed in a channel region within the active area. The sacrificial layer may comprise a layer of epitaxial SiGe for a p-MOS (e.g., $SiGe_{0.3}$), or a composite layer of epitaxial Si on layer of epitaxial SiGe for an n-MOS (e.g., $Si/SiGe_{0.2}$).

At step **1308** a gate dielectric is formed, which may comprise $SiO_2$ or a Hi-K dielectric to reduce power loss due to gate current leakage into the channel region.

At step **1310** a gate material is formed. The gate may comprise a layer of Poly-Silicon or metal above the layer of gate dielectric and subjects the substrate to thermal cycling (Hi T).

At step **1312** a gate spacer is formed, which may comprise a dielectric sidewall spacer to insure electrical isolation of the gate poly.

At step **1314** a lightly-doped drain (LDD) is formed to improve charge carrier movement within the channel region.

At step **1316** a LDD anneal is performed to further improve charge carrier movement through the channel region. At the same time a dummy spacer is formed. Both processes subject the substrate to thermal cycling (Hi T).

At step **1318** the sacrificial layer is removed to form a recess by a wet chemical etch, a dry chemical etch, or a combination thereof, that utilizes an isotropic etch profile.

At step **1320** a strain inducing layer or high mobility layer is formed in the recess. The strain inducing layer or high mobility layer may comprise a layer of epitaxial SiGe for a p-MOS (e.g., $SiGe_{0.3}$), a gradient concentration layer (e.g., Ge), a doped layer (e.g., Boron or Phosphorus), a composite layer of epitaxial Si on layer of epitaxial SiGe for an n-MOS (e.g., $Si/SiGe_{0.2}$), or any combination thereof.

FIG. **14** illustrates a flow diagram of some embodiments of a method **1400** for manufacturing a channel-last replacement channel. Note that the method **1400** is applicable only in the Hi-K metal gate last (HKL) flow. While method **1400** is illustrated and described below as a series of acts or events, it will be appreciated that the illustrated ordering of such acts or events are not to be interpreted in a limiting sense. For example, some acts may occur in different orders and/or concurrently with other acts or events apart from those illustrated and/or described herein. In addition, not all illustrated acts may be required to implement one or more aspects or embodiments of the description herein. Further, one or more of the acts depicted herein may be carried out in one or more separate acts and/or phases.

At step **1402** a substrate is provided. The substrate may comprise a 300 mm or 450 mm crystalline wafer comprising silicon that has been doped with boron, phosphorus, arsenic, or antimony.

At step **1404** an active area is formed, which may comprise doping of the substrate.

At step **1406** a sacrificial layer is formed in a channel region within the active area. The sacrificial layer may comprise a layer of epitaxial SiGe for a p-MOS (e.g., $SiGe_{0.3}$), or a composite layer of epitaxial Si on layer of epitaxial SiGe for an n-MOS (e.g., $Si/SiGe_{0.2}$).

At step **1408** a dummy gate liner (IL) is formed.

At step **1410** a dummy gate material is formed. The dummy gate may comprise a layer of dummy oxide beneath a dummy gate material (e.g., Poly-Silicon). The dummy gate is capped by a hard mask. The formation of the dummy gate subjects the substrate to thermal cycling (Hi T).

At step **1412** a gate spacer is formed, which may comprise a dielectric sidewall spacer to insure electrical isolation of the gate poly.

At step **1414** a lightly-doped drain (LDD) is formed to improve charge carrier movement within the channel region.

At step **1416** a LDD anneal is performed to further improve charge carrier movement within the channel region. The LDD anneal subjects the substrate to thermal cycling (Hi T).

At step **1418** a source and drain epi layer is formed. The source and drain epi layer may comprise a layer of epitaxial

SiGe for a p-MOS (e.g., $SiGe_{0.3}$), or a composite layer of epitaxial Si on layer of epitaxial SiGe for an n-MOS (e.g., $Si/SiGe_{0.2}$).

At step **1420** a source and drain implant and anneal is performed. The source and drain implant may comprise an ion implantation of arsenic to improve threshold voltage. The anneal subjects the substrate to thermal cycling (Hi T).

At step **1422** the hard mask is removed from above the gate, which may comprise a wet chemical etch, a dry chemical etch, or a combination thereof.

At step **1424** a contact etch stop layer is added above the gate, spacer, source, and drain. An interlayer dielectric (ILD) is added above the etch stop layer.

At step **1426** the contact etch stop layer and ILD are subjected to a chemical-mechanical polish (CMP) to expose the top of the dummy gate material.

At step **1428** the dummy gate material is removed, which may comprise a wet chemical etch, a dry chemical etch, or a combination thereof.

At step **1430** the dummy oxide is removed, which may comprise a wet chemical etch, a dry chemical etch, or a combination thereof.

At step **1432** the channel region is removed to form a recess. The removal of the channel region may comprise wet chemical etch, a dry chemical etch, or a combination thereof, that utilizes an isotropic etch profile, and anisotropic etch profile, a sigma-shape etch profile, or a triangular etch profile.

At step **1434** a strain inducing layer or high mobility layer is formed in the recess. The second strain inducing layer or high mobility layer may comprise a layer of epitaxial SiGe for a p-MOS (e.g., $SiGe_{0.3}$), a gradient concentration layer (e.g., Ge), a doped layer (e.g., Boron or Phosphorus), a composite layer of epitaxial Si on layer of epitaxial SiGe for an n-MOS (e.g., $Si/SiGe_{0.2}$), or any combination thereof.

FIG. **15***a*-FIG. **15***f* illustrate cross-sectional views of some embodiments of channel-last replacement channel profiles. FIG. **15***a* illustrates a cross-sectional view of some embodiments **1500***a* of a sigma-shape profile **1502***a* for a channel-last replacement channel. FIG. **15***b* illustrates a cross-sectional view of some embodiments **1500***b* of a sigma-shape profile **1502***b* for a channel-last replacement channel. FIG. **15***c* illustrates a cross-sectional view of some embodiments **1500***c* of an anisotropic profile **1502***c* for a channel-last replacement channel. FIG. **15***d* illustrates a cross-sectional view of some embodiments **1500***d* of an isotropic profile **1502***d* for a channel-last replacement channel. FIG. **15***e* illustrates a cross-sectional view of some embodiments **1500***e* of a triangular profile **1502***e* for a channel-last replacement channel. FIG. **15***f* illustrates a cross-sectional view of some embodiments **1500***f* of a trapezoidal profile **1502***f* for a channel-last replacement channel.

It will also be appreciated that equivalent alterations and/or modifications may occur to one of ordinary skill in the art based upon a reading and/or understanding of the specification and annexed drawings. The disclosure herein includes all such modifications and alterations and is generally not intended to be limited thereby. In addition, while a particular feature or aspect may have been disclosed with respect to only one of several implementations, such feature or aspect may be combined with one or more other features and/or aspects of other implementations as may be desired. Furthermore, to the extent that the terms "includes", "having", "has", "with", and/or variants thereof are used herein; such terms are intended to be inclusive in meaning—like "comprising." Also, "exemplary" is merely meant to mean an example, rather than the best. It is also to be appreciated that features, layers and/or elements depicted herein are illustrated with particular dimensions and/or orientations relative to one another for purposes of simplicity and ease of understanding, and that the actual dimensions and/or orientations may differ substantially from that illustrated herein.

Therefore, the present disclosure relates to a device and method for strain inducing or high mobility channel replacement in a semiconductor device. The semiconductor device is configured to control current from a source to a drain through a channel region by use of a gate. A sacrificial layer is formed early in the semiconductor device processing. After one or more thermal processing steps are carried out with the sacrificial layer in place, the sacrificial layer is removed to form a recess. A strain inducing or high mobility layer then fills the recess to insure a robust crystal structure with minimal defects. Strain inducing or high mobility channel replacement may result in better device performance compared to conventional techniques for strain inducing channel formation, and is fully compatible with the current semiconductor manufacturing infrastructure.

In some embodiments, the strain inducing or high mobility channel replacement comprises a partial replacement channel on a field effect transistor (FET), wherein a sacrificial layer forming a source, drain, and channel region are removed after a series of thermal processing steps to form a recess. The recess is then with a strain inducing or high mobility layer. These embodiments comprise a partially removing the sacrificial layer such that a portion of the sacrificial layer remains immediately below the gate. This results in a partial replacement channel that is a combination of the sacrificial layer and the strain inducing or high mobility layer.

In some embodiments, the strain inducing channel replacement comprises a full replacement channel on a field effect transistor (FET), wherein a sacrificial layer forming a source, drain, and channel region are removed after a series of thermal processing steps to form a recess. The recess is then with a strain inducing or high mobility layer. These embodiments comprise a fully removing the sacrificial layer such that none of the sacrificial layer remains above the source, drain, and channel region. This results in a full replacement channel comprising only the strain inducing or high mobility layer.

In some embodiments the present disclosure relates to a method for strain inducing or high mobility channel replacement comprising partially replacing a channel on a field effect transistor (FET), wherein a sacrificial layer forms a source, drain, and channel region. After a series of thermal processing steps are performed, the sacrificial layer is removed to form a recess. The recess is then filled with a strain inducing or high mobility layer. In the method of these embodiments the sacrificial layer is partially removed such that a portion of the sacrificial layer remains immediately below the gate. The removed portion of the sacrificial layer is then replaced with a strain inducing or high mobility layer such that the replacement channel is a combination of the sacrificial layer and the strain inducing or high mobility layer.

In some embodiments the present disclosure relates to a method for strain inducing channel replacement comprising fully replacing a channel on a field effect transistor (FET), wherein a sacrificial layer forms a source, drain, and channel region. After a series of thermal processing steps are performed, the sacrificial layer is removed to form a recess. The recess is then filled with a strain inducing or high mobility layer. In the method of these embodiments the sacrificial layer is fully removed such that none of the sacrificial layer remains above the source, drain, and channel region. The removed sacrificial layer is then replaced with a strain inducing or high mobility layer such that the replacement channel comprises only the strain inducing or high mobility layer.

What is claimed is:

1. A semiconductor device, comprising:

a continuous strain inducing or high mobility layer arranged within a recess in an upper surface of a substrate and configured to provide increased charge carrier mobility relative to the substrate;

a gate arranged over the continuous strain inducing or high mobility layer, and separated from the continuous strain inducing or high mobility layer by a dielectric;

a channel region arranged within the continuous strain inducing or high mobility layer and arranged under the gate;

doped source/drain regions arranged within the continuous strain inducing or high mobility layer and laterally separated from one another by the channel region; and

a low mobility layer confined to directly over the channel region and separating an underside of the gate from the channel region, wherein the low mobility layer has a different semiconductor lattice than the substrate.

**2**. The semiconductor device of claim **1**, wherein the doped source/drain regions comprise raised source/drain regions, which extend above an upper surface of the substrate.

**3**. The semiconductor device of claim **2**, wherein the raised source/drain regions have a diamond shaped cross-section along a channel length direction of the continuous strain inducing or high mobility layer.

**4**. The semiconductor device of claim **2**, wherein the raised source/drain regions have a hexagonal shaped cross-section along a channel length direction of the continuous strain inducing or high mobility layer.

**5**. The semiconductor device of claim **2**, wherein the raised source/drain regions have an octagonal shaped cross-section along a channel length direction of the continuous strain inducing or high mobility layer.

**6**. The semiconductor device of claim **2**, wherein the raised source/drain regions have an isotropic shaped cross-section along a channel length direction of the continuous strain inducing or high mobility layer.

**7**. A semiconductor device, comprising:

a fin which protrudes from an upper surface of a semiconductor substrate and which comprises a fin region of a continuous strain inducing or high mobility layer which is configured to provide increased charge carrier mobility relative to the semiconductor substrate;

a gate, which straddles a channel region disposed within the fin, and which is separated from the continuous strain inducing or high mobility layer by a dielectric;

doped source/drain regions disposed in the continuous strain inducing or high mobility layer, and which are laterally separated from one another by the channel region; and

a sacrificial layer arranged within an opening in an upper surface of the semiconductor substrate, under the continuous strain inducing or high mobility layer, and wherein the sacrificial layer and the continuous strain inducing or high mobility layer have a same width.

**8**. The semiconductor device of claim **7**, wherein the fin further comprises:

a low mobility layer confined to the channel region and arranged over the continuous strain inducting or high mobility layer, wherein the low mobility layer separates an underside of the gate from the channel region and shares a crystalline structure with the sacrificial layer.

**9**. The semiconductor device of claim **7**,

wherein the continuous strain inducing or high mobility layer comprises a heterostructure comprising one or more layers of Si and one or more layers SiGe; and

wherein the channel region is arranged within the one or more layers of Si.

**10**. The semiconductor device of claim **7**, wherein the gate comprises metal.

**11**. A semiconductor device, comprising:

source/drain regions comprising strain inducing or high mobility layers disposed on a semiconductor substrate;

a gate disposed over the semiconductor substrate and disposed between the source/drain regions; and

a channel region disposed under the gate and separating the source/drain regions from one another, wherein the channel region includes:

 a first channel layer having a lower surface recessed below an upper surface of the semiconductor substrate and extending continuously between the source/drain regions, wherein the first channel layer is distinct from the semiconductor substrate; and

 a second channel layer disposed in a recess within the first channel layer, wherein the first channel layer exhibits an increased carrier mobility relative to the semiconductor substrate, wherein the first and second channel layers are structurally distinct from one another, and wherein opposite sidewalls of the recess are laterally spaced from the source/drain regions.

**12**. The semiconductor device of claim **11**, wherein the second channel layer is arranged directly below the gate such that vertical sidewalls of the gate and vertical sidewalls of the second channel layer are aligned with one another.

**13**. The semiconductor device of claim **11**, wherein the first channel layer comprises a heterostructure comprising alternating horizontal layers of Si and SiGe.

**14**. The semiconductor device of claim **1**, wherein the first channel layer is made of silicon or silicon germanium and wherein the second channel layer is made of silicon germanium or germanium.

**15**. The semiconductor device of claim **11**, wherein the second channel layer has a lower density of lattice defects or a more tightly controlled doping profile than the first channel layer.

**16**. The semiconductor device of claim **11**, wherein the first and second channel layers comprise first and second materials which have different lattice constants from one another.

**17**. The semiconductor device of claim **11**, wherein the source/drain regions comprise raised source/drain regions, which extend above the upper surface of the semiconductor substrate.

**18**. The semiconductor device of claim **11**, wherein the recess in the first channel layer has a rectangular cross-section, u-shaped cross-section, v-shaped cross-section, a hexagonal-shaped cross-section, or an octagonal-shaped cross-section.

**19**. The semiconductor device of claim **11**, wherein the channel region is disposed within a fin, which protrudes from an upper surface of the semiconductor substrate, and wherein the gate straddles the channel region.

**20**. The semiconductor device of claim **1**, further comprising:

a sacrificial layer arranged in the recess, under the continuous strain inducing or high mobility layer, wherein the sacrificial layer shares a crystalline structure with the low mobility layer.

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